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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/666,564	09/19/2003	Katherine L. Saenger	YOR90030274US1	5537

7590 06/16/2005

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EXAMINER	
WILLIAMS, ALEXANDER O	
ART UNIT	**PAPER NUMBER**
2826	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/666,564	SAENGER ET AL.	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *28 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) *2-33* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *9/19/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/666564 Attorney's Docket #: YOR920030274 US1
Filing Date: 9/19/2003;

Applicant: Saenger et al.

Examiner: Alexander Williams

Applicant's election of species I (claim 1), filed 3/28/05, has been acknowledged.

This application contains claims 2 to 33 drawn to an invention non-elected with traverse.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Applicant is reminded of the proper content of an abstract of the disclosure.

A patent abstract is a concise statement of the technical disclosure of the patent and should include that which is new in the art to which the invention pertains. If the patent is of a basic nature, the entire technical disclosure may be new in the art, and the abstract should be directed to the entire disclosure. If the patent is in the nature of an improvement in an old apparatus, process, product, or composition, the abstract should include the technical disclosure of the improvement. In certain patents, particularly those for compounds and compositions, wherein the process for making and/or the use thereof are not obvious, the abstract should set forth a process for making and/or use thereof. If the new technical disclosure involves modifications or alternatives, the abstract should mention by way of example the preferred modification or alternative.

The abstract should not refer to purported merits or speculative applications of the invention and should not compare the invention with the prior art.

Where applicable, the abstract should include the following:
(1) if a machine or apparatus, its organization and operation;
(2) if an article, its method of making;

(3) if a chemical compound, its identity and use;
(4) if a mixture, its ingredients;
(5) if a process, the steps.

Extensive mechanical and design details of apparatus should not be given.

Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

The use of the trademark on pages 3 and 25 of the specification and throughout the specification has been noted in this application. It should be capitalized wherever it appears and be accompanied by the generic terminology.

Although the use of trademarks is permissible in patent applications, the proprietary nature of the marks should be respected and every effort made to prevent their use in any manner which might adversely affect their validity as trademarks.

The disclosure is objected to because of the following informalities: On [age 27, line 21, it is unclear what number represent “a thin conformal conductive liner.” The number of 2130 appear to have a line through it canceling out the number. Should there be a number in its replacement for the liner?

Appropriate correction is required.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. § 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless --

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by Kloster et al. (U.S. Patent Application Publication # 2004/0214427 A1).

1. Kloster et al. (figures 1A to 1J) specifically figure 1C show a closed air gap interconnect structure comprising: at least two conductive interconnect lines 102 separated by an air gap 105, wherein at least one of said lines is connected to at least one conducting via 102, wherein said lines are supported underneath by a plurality of regions 104 made of a robust support dielectric and capped on top by a cap layer 106.

DOCUMENT-IDENTIFIER: US 20040214427 A1

TITLE: Forming thin hard mask over air gap or porous dielectric

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Detail Description Paragraph - DETX (2):

[0010] Set forth below is a description of embodiments of the present invention, presented in the context of a semiconductor device that includes copper containing dual damascene interconnects. The description is made with reference to FIGS. 1a-1j which illustrate cross-sections of structures that result after using certain steps according to certain embodiments of the invention. Although dual damascene interconnects are described, it will be understood that the present invention also may be used in the context of other semiconductor devices, including but not limited to single damascene processes, in which one or more hard mask layers may be formed immediately over and/or adjacent an air gap or dielectric layer.

Detail Description Paragraph - DETX (4):

[0012] Such conductive layers may comprise copper, and may be formed using a conventional copper electroplating process, in which a copper layer is formed on barrier and seed layers. A conductive layer or layers also may be made from other materials conventionally used to form conductive layers for integrated circuits. For example, conductive layers may be made from a copper alloy, aluminum or an aluminum alloy, such as an aluminum/copper alloy. Alternatively, they may be made from doped polysilicon silicide, e.g., a silicide comprising tungsten, titanium, nickel or cobalt. The substrate also may comprise a primary conductor made from an aluminum/copper alloy that is sandwiched between a relatively thin titanium

layer located below it and a titanium, titanium nitride double layer above it.

Detail Description Paragraph - DETX (6):

[0014] Substrate 100 also may include a barrier layer made from silicon nitride, silicon carbide or other materials such as titanium nitride or oxynitride, as is well known to those skilled in the art. When formed from silicon nitride, a chemical vapor deposition process may be used to form the barrier layer. A barrier layer may serve to prevent an unacceptable amount of copper, or other metal, from diffusing into other layers, and also may act as an etch stop to prevent subsequent via and trench etch steps from exposing an underlying conductive layer to subsequent cleaning steps. The barrier layer should be thick enough to perform its diffusion inhibition and etch stop functions, but not so thick that it adversely impacts. The overall dielectric characteristics resulting from the combination of the barrier layer and the dielectric layer overlying the barrier layer. The thickness of the barrier layer preferably should be less than about 10% of the thickness of the overlying dielectric layer, and preferably between about 100 and 500 angstroms thick.

Detail Description Paragraph - DETX (24):

[0032] An example of a pore-filling material for use third embodiment is 4 mercapto-n-butyltrimethoxysilane, which may be used to seal pores in oxides by reaction of Si--OCH.sub.3 with surface Si--OH groups, followed by condensation of remaining Si--OCH.sub.3 groups. The thiol end cap provides a site which can be crosslinked under mild oxidation conditions that do not oxidize copper. The sulfur also provides some polarity to enhance barrier nucleation, if desired.

Detail Description Paragraph - DETX (25):

[0033] Another example of a pore filling material in the third embodiment is 3-methoxypropyltrimethoxysilane, which may be used to seal pores in oxides by reaction of Si--OCH.sub.3 with surface Si--OH groups, followed by condensation of remaining Si--OCH.sub.3 groups. Polar methoxypropyl enhances nucleation of the barrier metal layer.

Detail Description Paragraph - DETX (29):

[0037] The trench and via may be filled with conductive material to form metal traces 102. The conductive material may

be copper, tungsten, aluminum, silver, gold, and their respective alloys. A CMP step may be used to remove excess conductive material and planarize the top surface of the metal traces. Optionally, a metal diffusion shunt or metal barrier layer 106 may be formed over each of the metal traces.

Claim 1 is rejected under 35 U.S.C. § 102(e) as being anticipated by Morrow et al. (U.S. Patent # 6,661,094 B2).

1. Morrow et al. (figures 1 to 6C) specifically figure 3 show a closed air gap interconnect structure comprising: at least two conductive interconnect lines 350,318 separated by an air gap 323, wherein at least one of said lines is connected to at least one conducting via 318,350, wherein said lines are supported underneath by a plurality of regions (should as 102 in figure 1) made of a robust support dielectric and capped on top by a cap layer 320.

Claim 1 is rejected under 35 U.S.C. § 102(b) as being anticipated by Lee (U.S. Patent # 6,277,705 B1).

1. Lee (figures 1A to 2) specifically figure 2F show a closed air gap interconnect structure comprising: at least two conductive interconnect lines 22 separated by an air gap 26b, wherein at least one of said lines is connected to at least one conducting via 22, wherein said lines are supported underneath by a plurality of regions 20 made of a robust support dielectric and capped on top by a cap layer 24.

US-PAT-NO: 6277705

(11) SUMMARY OF THE INVENTION

(12) Based on the foregoing, the present invention provides a fabrication method for forming an air-gap using a hard mask. The hard mask layer is used to increase the etching selectivity on the dielectric layer to form an opening with a high aspect ratio. The space occupied by the hard mask layer is further used to form an air-gap after the removal of the hard mask layer.

(13) The present invention provides a fabrication method for forming an air-gap using a hard mask, which method is applicable on a semiconductor substrate. The semiconductor substrate comprises a first conductive layer, for example, a source/drain region of a metal oxide semiconductor (MOS) or a metal interconnect, wherein a dielectric layer is formed on the first conductive layer. The fabrication method according to the present invention includes forming a patterned hard mask layer on the dielectric layer. A portion of the dielectric layer is removed to form an opening in the dielectric layer and to expose the first conductive layer while using the patterned hard mask layer as a mask. A conductive material then fills the opening, forming a conductive plug in the dielectric layer to electrically connect with the first conductive layer. After this, a second conductive layer is formed on the hard mask layer, covering the conductive plug and electrically connecting to the conductive plug. The hard mask layer is then removed, followed by forming a poor step coverage silicon oxide layer, for example, a plasma enhanced silicon oxide layer, to cover the substrate. An air-gap is further formed between the second conductive layer and the dielectric layer to reduce the parasitic capacitance.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/774,700,701,758751,760,750,759,522,618	6/11/05
Other Documentation: foreign patents and literature in 257/774,700,701,758751,760,750,759,522,618	6/11/05
Electronic data base(s): U.S. Patents EAST	6/11/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
6/11/05